Automatic application-specific instruction-set extensions under microarchitectural constraints

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Proceedings of the 40th annual Design Automation Conference table of contents
Anaheim, CA, USA
SESSION: Issues in partitioning & design space eploration for codesign table of contents
Pages: 256 - 261
Year of Publication: 2003
ISBN:1-58113-688-9

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Sponsor ACM: Association for Computing Machinery

Publisher ACM New York, NY, USA

DOI Bookmark: Use this link to bookmark this Article: http://doi.acm.org/10.1145/775832.775897
What is a DOI?

ABSTRACT

Many commercial processors now offer the possibility of extending their instruction set for a specific application---that is, to introduce customised functional units. There is a need to develop algorithms that decide automatically, from high-level application code, which operations are to be carried out in the customised extensions. A few algorithms exist but are severely limited in the type of operation clusters they can choose and hence reduce significantly the effectiveness of specialisation. In this paper we introduce a more general algorithm which selects maximal-speedup convex subgraphs of the application dataflow graph under fundamental microarchitectural constraints, and which improves significantly on the state of the art.

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INDEX TERMS

Primary Classification:

C. Computer Systems Organization

C.1 PROCESSOR ARCHITECTURES

C.1.3 Other Architecture Styles

General Terms:

Algorithms, Design, Performance

Keywords:

ASIPs, codesign, customisable processors, instruction-set extensions

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